IDF13

NVM Express:
Optimized Interface for PCI Express SSDs*

Amber Huffman – Sr. Principal Engineer, Intel Corporation

SSDS004

intel Look Inside.

Agenda

- Why NVM Express?
- Overview of NVM Express (NVMe)
- New Technical Developments in NVMe
- Driver Ecosystem Update
- Real NVMe Solutions

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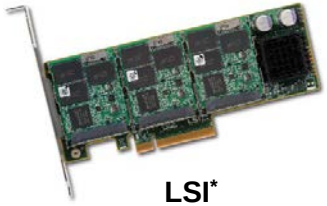
PCI Express* for Datacenter/Enterprise SSDs

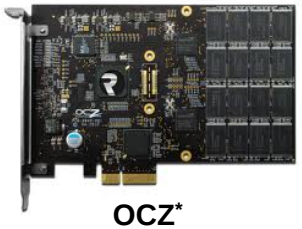
- PCI Express* (PCIe) is a great interface for SSDs
  - Stunning performance — 1 GB/s per lane (PCIe Gen3 x1)
  - With PCIe scalability — 8 GB/s per device (PCIe Gen3 x8) or more
  - Lower latency — Platform+Adapter: 10 µsec down to 3 µsec
  - Lower power — No external SAS IOC saves 7-10 W
  - Lower cost — No external SAS IOC saves ~ $15
  - PCIe lanes off the CPU — 40 Gen3 (**80** in dual socket)

Virident*

Fusion-io*



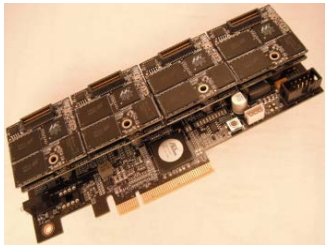
LSI*



OCZ*

Micron*

Intel



Marvell*

PCIe SSDs are emerging in Datacenter/Enterprise, co-existing with SAS & SATA depending on application

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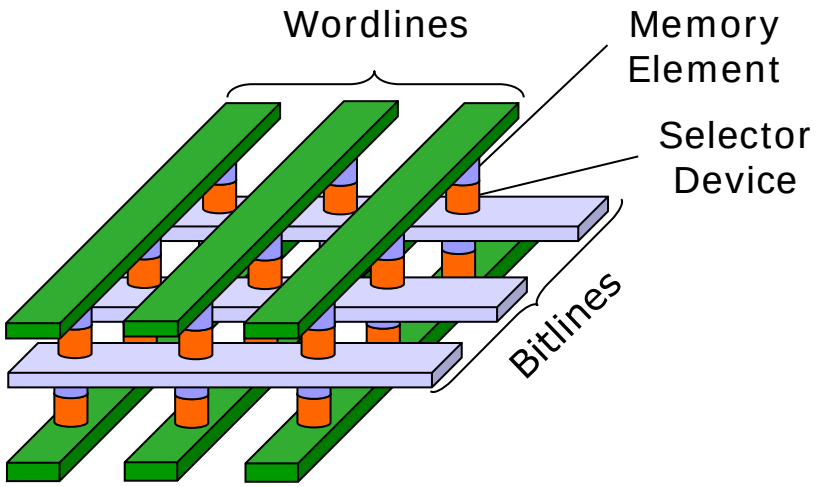
Next Generation Scalable NVM

Scalable Resistive Memory Element



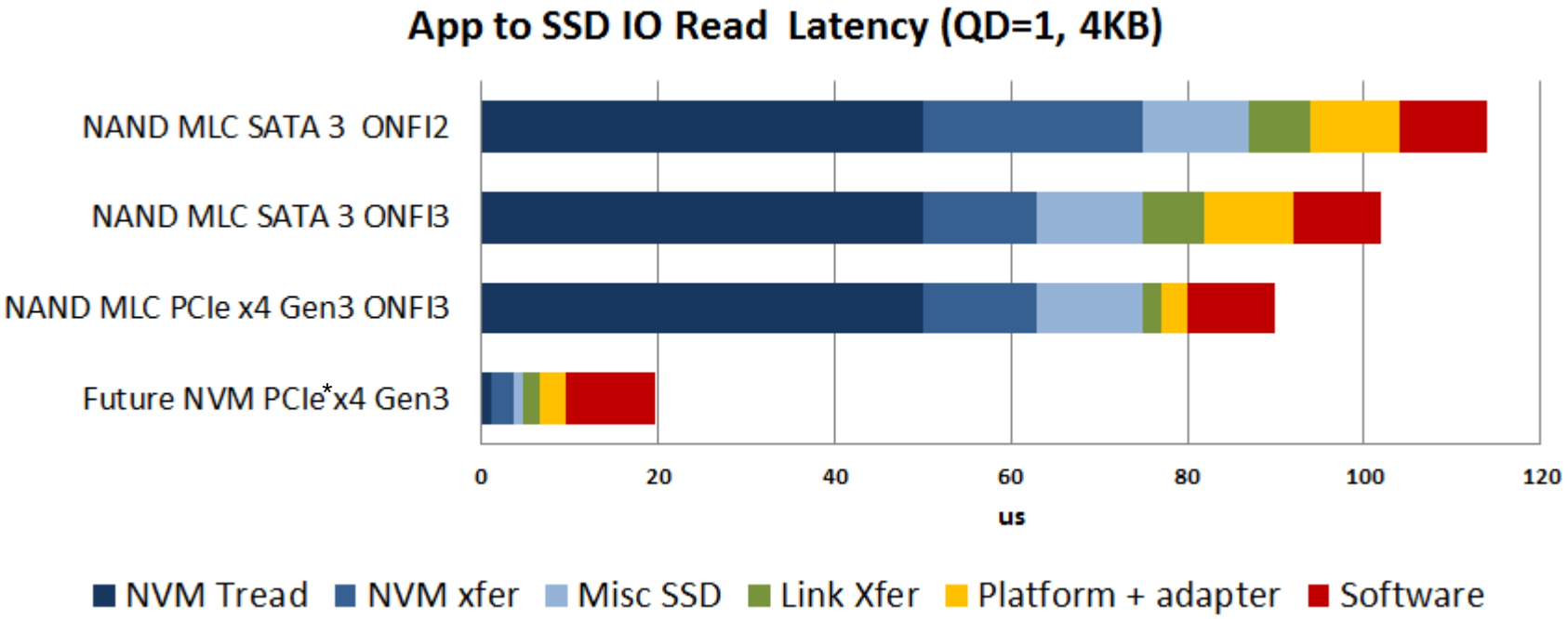
Cross Point Array in Backend Layers ~$4l^2$ Cell

Resistive RAM NVM Options

Family	Defining Switching Characteristics
Phase Change Memory	Energy (heat) converts material between crystalline (conductive) and amorphous (resistive) phases
Magnetic Tunnel Junction (MTJ)	Switching of magnetic resistive layer by spin-polarized electrons
Electrochemical Cells (ECM)	Formation / dissolution of "nano-bridge" by electrochemistry
Binary Oxide Filament Cells	Reversible filament formation by Oxidation-Reduction
Interfacial Switching	Oxygen vacancy drift diffusion induced barrier modulation

Many candidate next generation NVM technologies. Offer ~ 1000x speed-up over NAND.

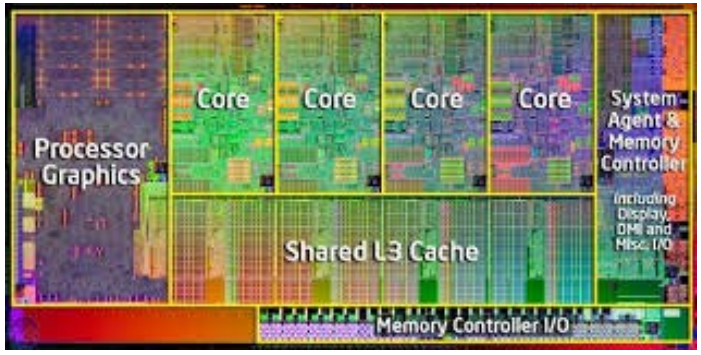
Fully Exploiting Next Generation NVM



- With Next Generation NVM, the NVM is no longer the bottleneck
  - Need optimized platform storage interconnect
  - Need optimized software storage access methods

Transformation Required

- Transformation was needed for full benefits of multi-core CPU
  - Application and OS level changes required



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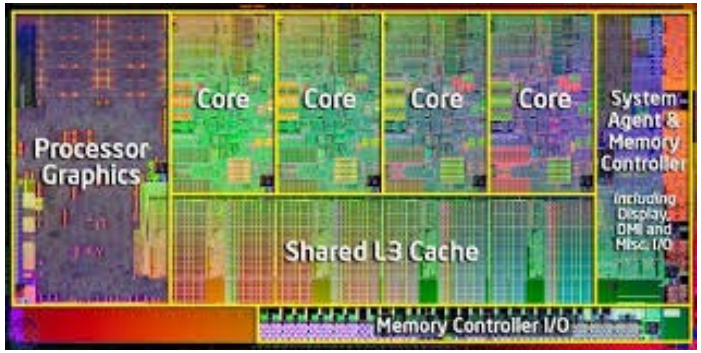
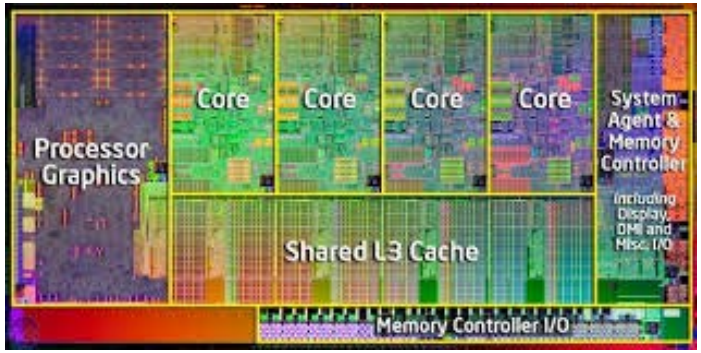
- To date, SSDs have used the legacy interfaces of hard drives
  - Based on a single, slow rotating platter



Transformation Required

- Transformation was needed for full benefits of multi-core CPU
  - Application and OS level changes required
- To date, SSDs have used the legacy interfaces of hard drives
  - Based on a single, slow rotating platter
- SSDs are inherently parallel and next gen NVM approaches DRAM-like latencies
- For full SSD benefits, must architect for NVM from the ground up



NVM Express* is the interface architected for NAND today and next generation NVM

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NVM Express* Overview

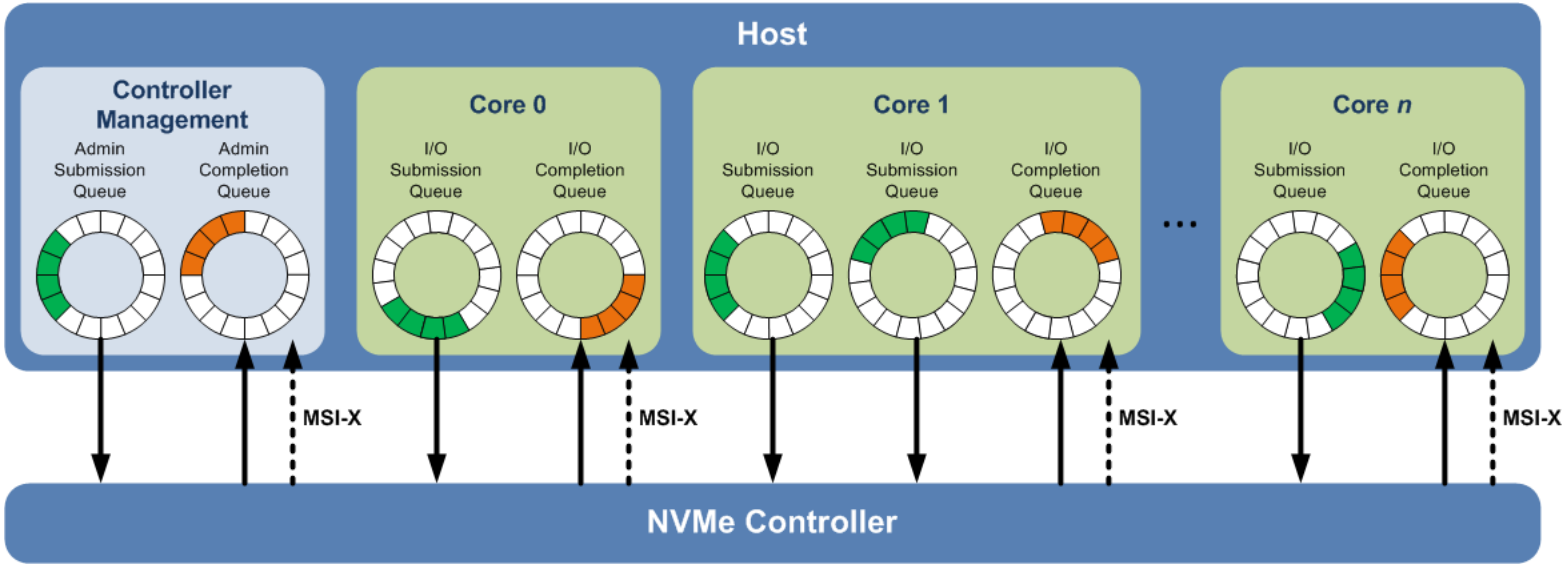
- NVM Express* (NVMe) is the standardized high performance host controller interface for PCI Express* SSDs

- NVMe was architected from the ground up for non-volatile memory, scaling from enterprise to client
  - The architecture focuses on latency, parallelism/performance, low power
  - The interface is explicitly designed with next generation NVM in mind

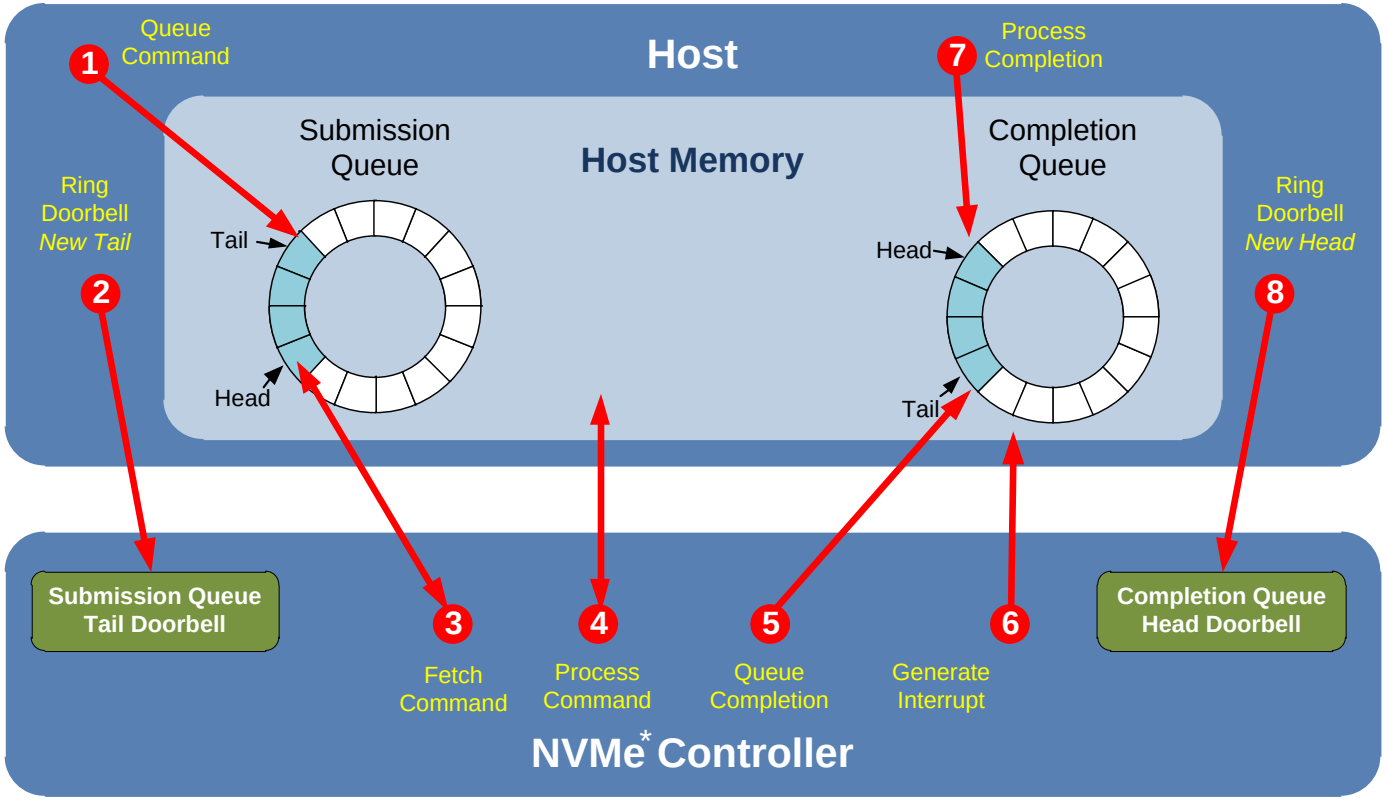
- NVMe was developed by an open industry consortium of 90+ members and is directed by a 13 company Promoter Group

Technical Basics

- All parameters for 4KB command in single 64B command
- Supports deep queues (64K commands per queue, up to 64K queues)
- Supports MSI-X and interrupt steering
- Streamlined & simple command set (13 required commands)
- Optional features to address target segment (Client, Enterprise, etc.)
  - Enterprise: End-to-end data protection, reservations, etc.
  - Client: Autonomous power state transitions, etc.
- Designed to scale for next generation NVM, agnostic to NVM type used



Queuing Interface
Command Submission & Processing



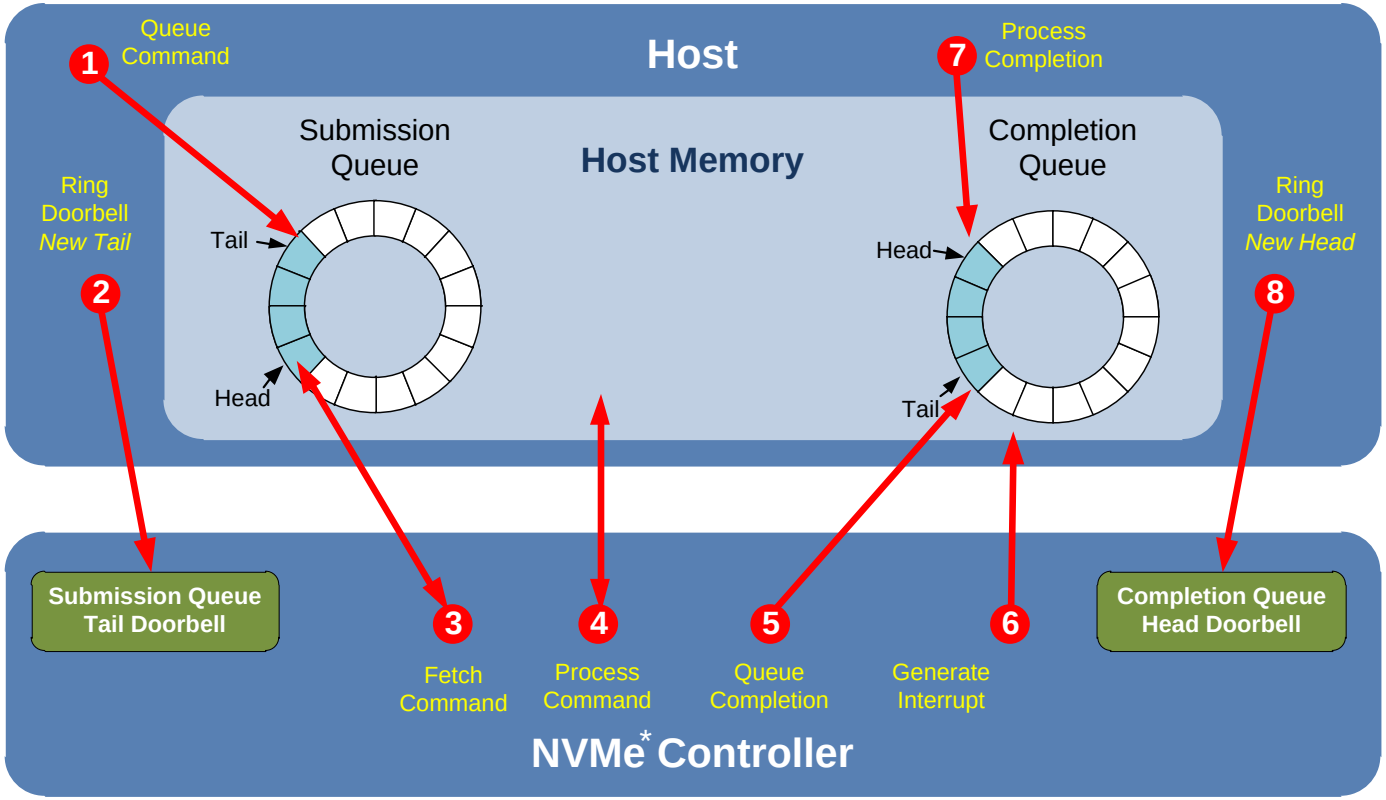
Command Submission

1. Host writes command to Submission Queue
2. Host writes updated Submission Queue tail pointer to doorbell

Command Processing

3. Controller fetches command
4. Controller processes command

Queuing Interface
Command Completion



Command Completion

5. Controller writes completion to Completion Queue
6. Controller generates MSI-X interrupt
7. Host processes completion
8. Host writes updated Completion Queue head pointer to doorbell

Simple Command Set – Optimized for NVM

Admin Commands
Create I/O Submission Queue
Delete I/O Submission Queue
Create I/O Completion Queue
Delete I/O Completion Queue
Get Log Page
Identify
Abort
Set Features
Get Features
Asynchronous Event Request
Firmware Activate (optional)
Firmware Image Download (opt)
Format NVM (optional)
Security Send (optional)
Security Receive (optional)

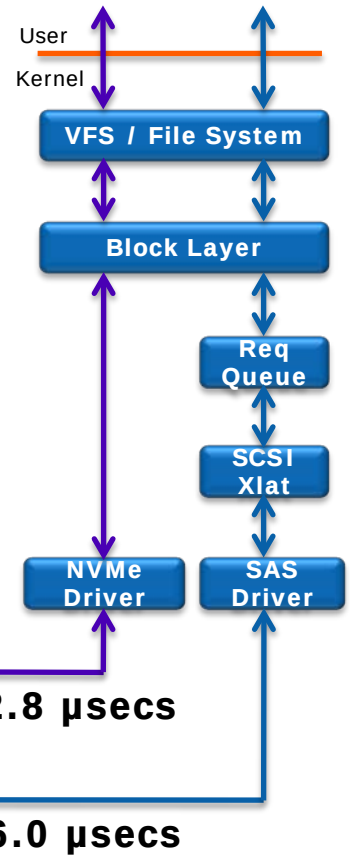
NVM I/O Commands
Read
Write
Flush
Write Uncorrectable (optional)
Compare (optional)
Dataset Management (optional)
Write Zeros (optional)
Reservation Register (optional)
Reservation Report (optional)
Reservation Acquire (optional)
Reservation Release (optional)

Only 10 Admin and 3 I/O commands required

Proof Point: NVM Express* Latency

- NVM Express* (NVMe) is designed to scale for next gen NVM
- NVMe reduces software overhead by over 50%
  - SCSI/SAS: 6.0 µs 19,500 cycles
  - **NVMe: 2.8 µs 9,100 cycles**
- Increased focus on storage stack / OS needed to reduce latency even further

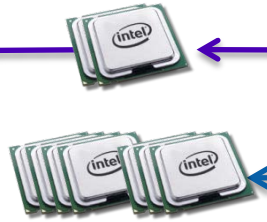
Linux* Storage Stack



Chatham NVMe Prototype

Prototype Measured IOPS

Cores Used for 1M IOPs



Measurement taken on Intel® Core™ i5-2500K 3.3GHz 6MB L3 Cache Quad-Core Desktop Processor using Linux RedHat* EL6.0 2.6.32-71 Kernel.

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NVM Express* 1.1 Overview

- The NVM Express 1.1 specification, published in October of 2012, adds additional optional client and Enterprise features

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- Reservations
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Power Optimizations
- Autonomous Power State Transitions

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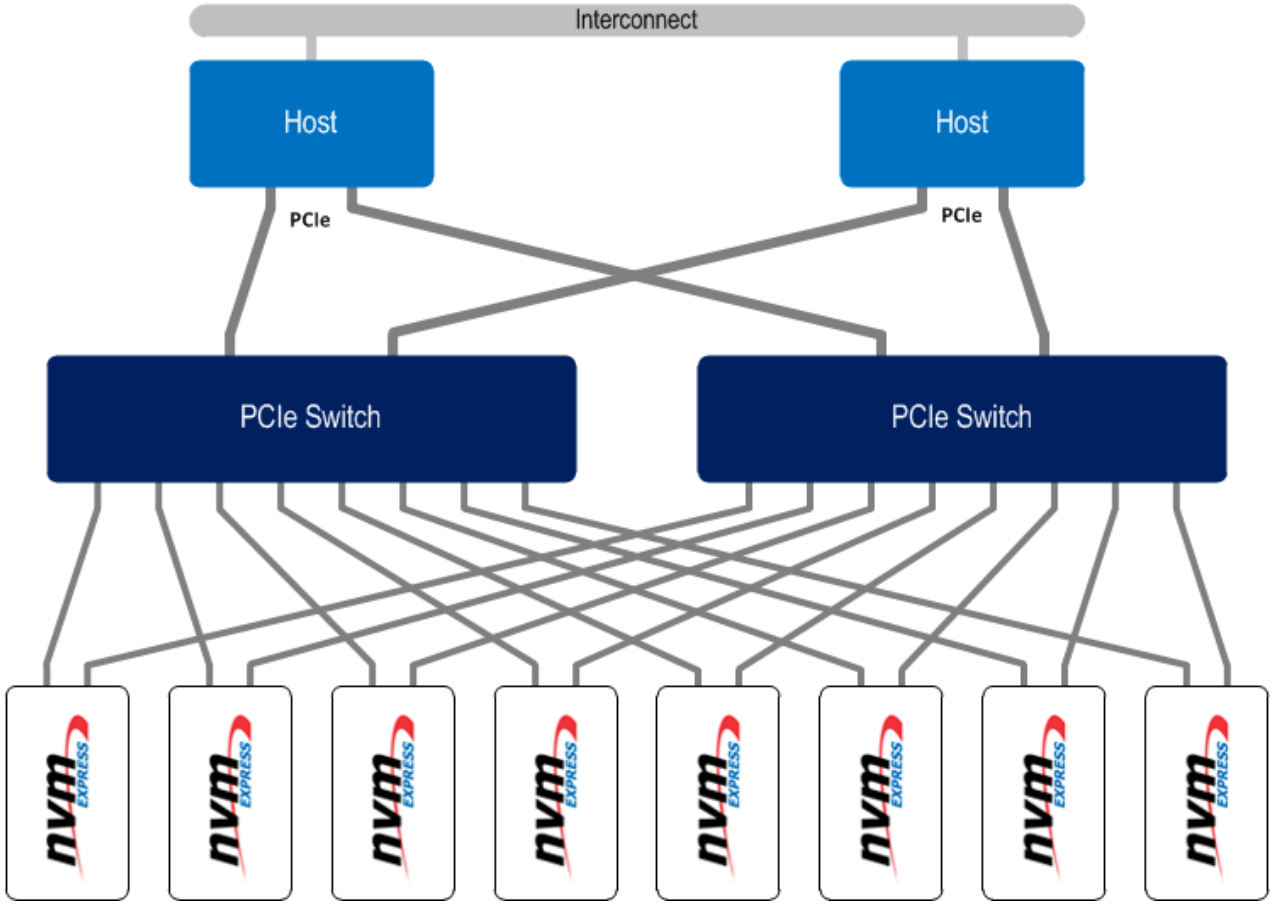
Command Enhancements
- Scatter Gather List support
- Active Namespace Reporting
- Persistent Features Across Power States
- Write Zeros Command

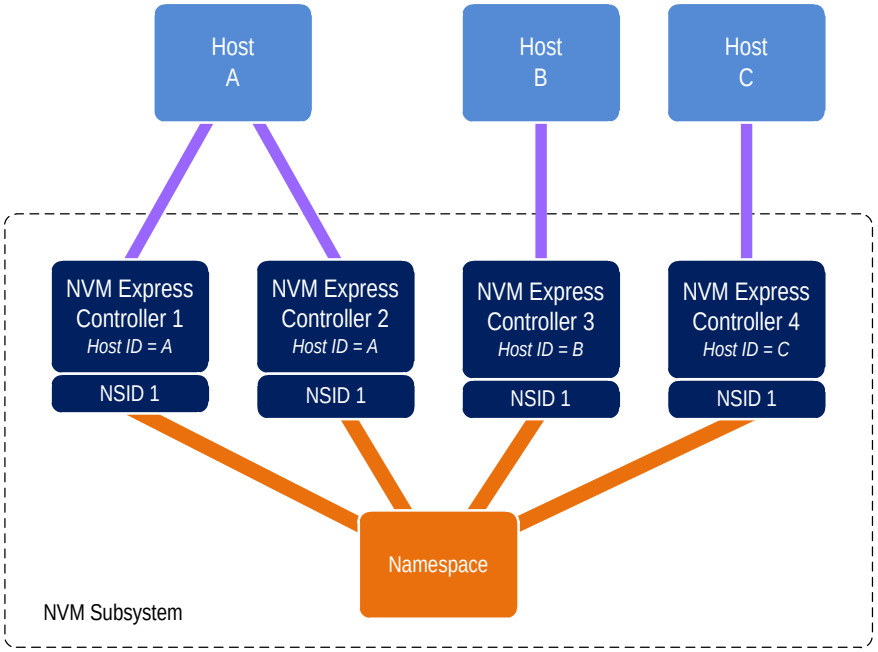
Multi-path Support

- Multi-path includes the traditional dual port model
- With PCI Express*, it extends further with switches



Reservations

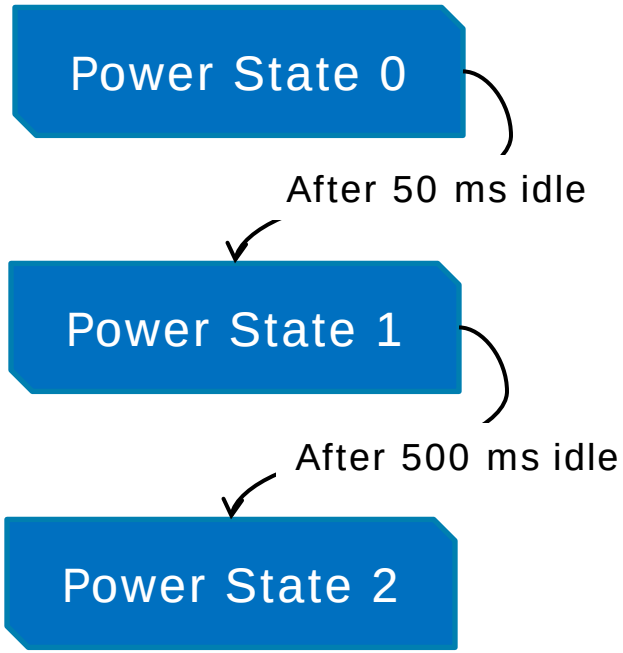
- In some multi-host environments, like Windows* clusters, reservations may be used to coordinate host access
- NVMe 1.1 includes a simplified reservations mechanism that is compatible with implementations that use SCSI reservations
- What is a reservation? Enables two or more hosts to coordinate access to a shared namespace.
  - A reservation may allow Host A and Host B access, but disallow Host C



Power Optimizations

- NVMe 1.1 added the Autonomous Power State Transition feature for client power focused implementations

- Without software intervention, the NVMe controller transitions to a lower power state after a certain idle period
  - Idle period prior to transition programmed by software



Example Power States

Power State	Opera-tional?	Max Power	Entrance Latency	Exit Latency
0	Yes	4 W	10 µs	10 µs
1	No	10 mW	10 ms	5 ms
2	No	1 mW	15 ms	30 ms

Continuing to Advance NVM Express*

- NVM Express continues to add features to meet the needs of client and Enterprise market segments as they evolve
- The Workgroup is defining features for the next revision of the specification, expected ~ middle of 2014

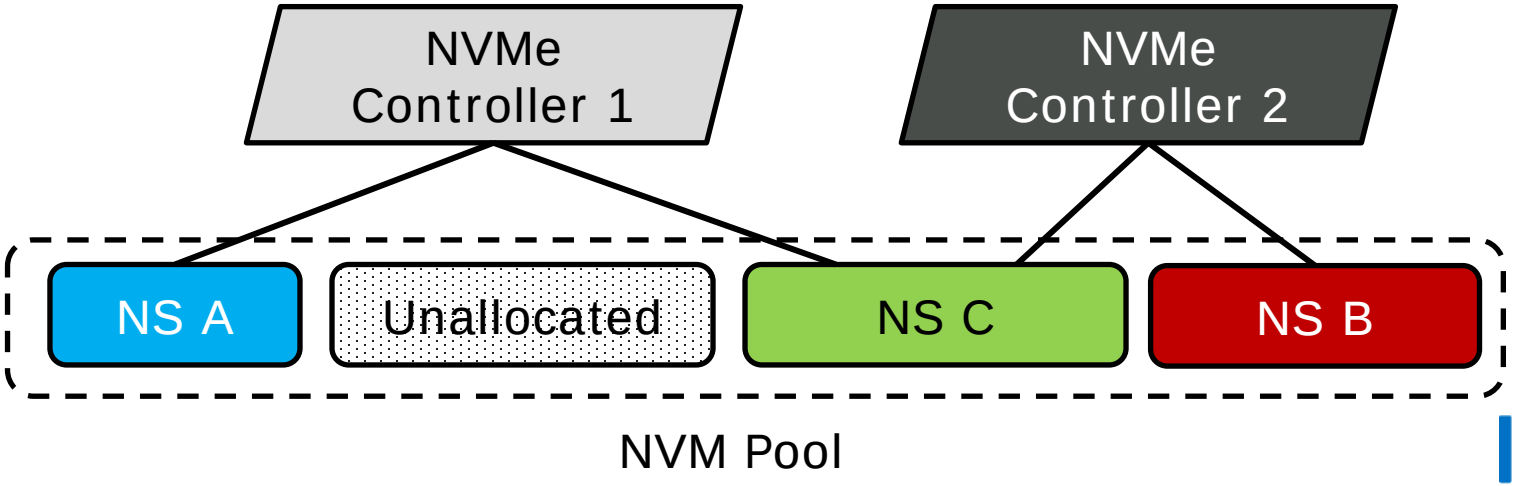
Features for Next Revision
Namespace Management
Live Firmware Update
Power Optimizations
Enhanced Status Reporting
Events for Namespace Changes
…

nvmexpress.org

Get involved – join the NVMe Workgroup.

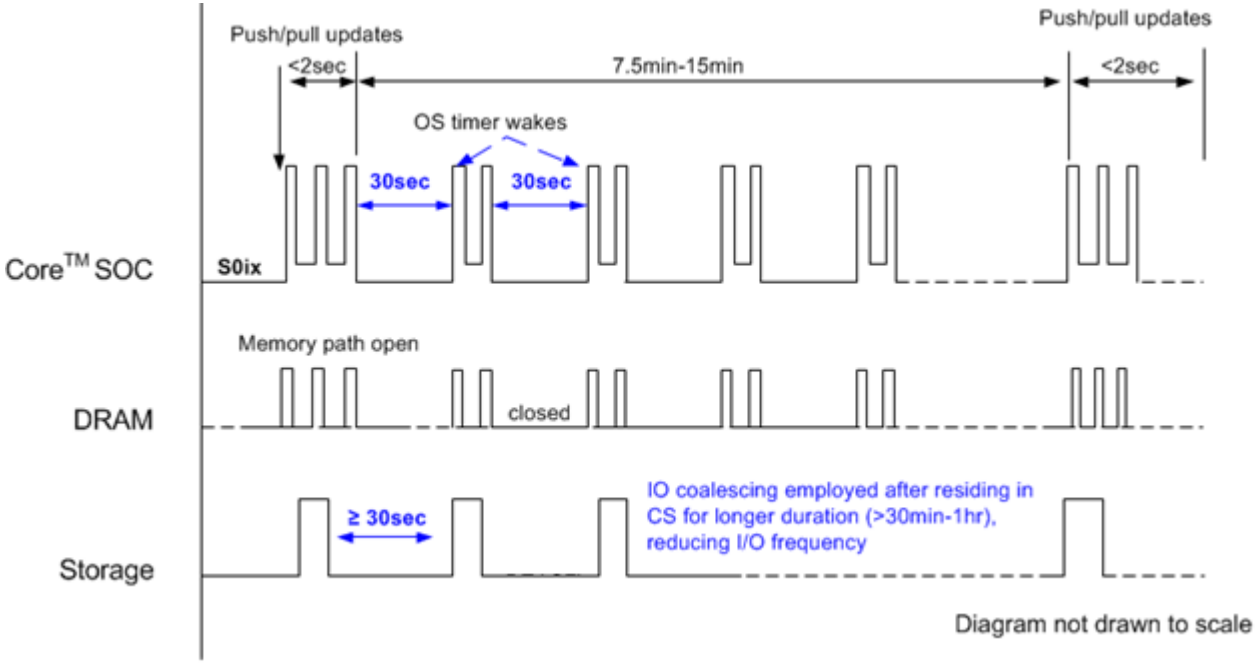
Future: Namespace Management

- A ***namespace*** is a pool of NVM exposed as logical blocks
- The management of namespaces (creation, deletion, resizing, etc) has been outside the scope of the specification
- Based on OEM feedback, the Workgroup is standardizing namespace management functions, including:
  - Create, delete, re-size (larger or smaller)
  - Ability to attach or detach a namespace to/from a controller
  - Reporting of namespace & NVM pool status, including namespaces that exist, amount of unallocated space in NVM pool, etc



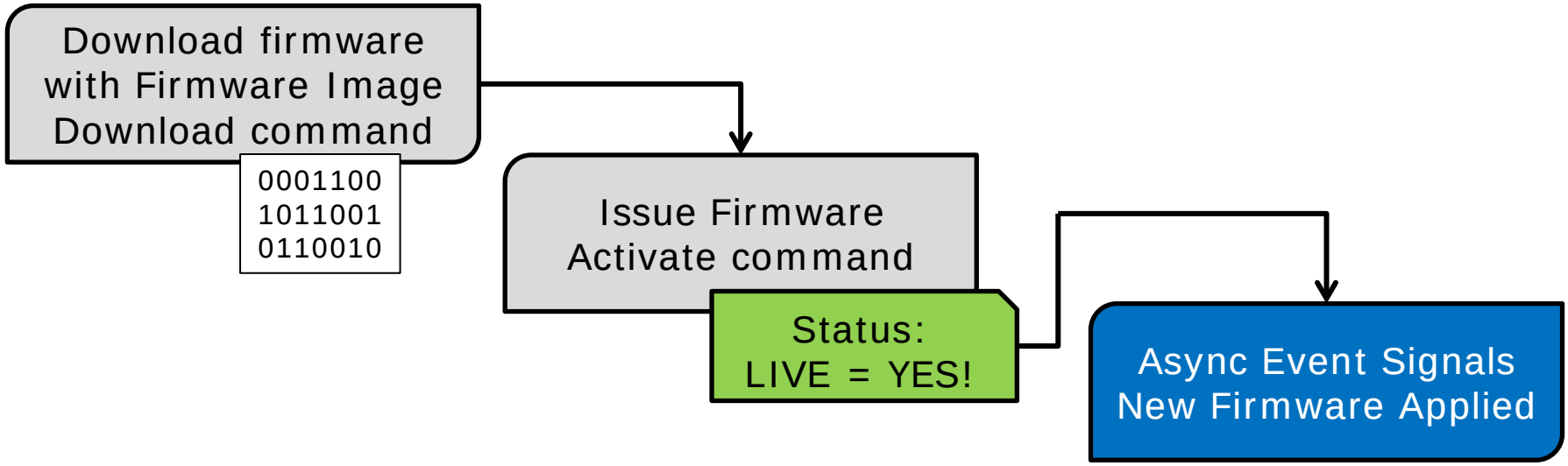
Future: Power Optimizations

- For best results, power policy needs to be tailored to the workload
- As an example, look at the Connected Standby (CS) workload:
  - All storage traffic is contained within 500 ms bursts
  - Bursts of storage traffic are every 30 seconds
  - Need good performance in burst, then immediate entry into deep sleep state
- A future enhancement is to convey workload information to the device



Future: “Live” Firmware Update

- The firmware update process requires a reset of the controller in order for the new firmware to be applied
- As part of the reset, the controller has to be re-initialized – queues have to be re-created and commands re-issued
- OEMs would like an option for “live” firmware update without a reset



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Driver Development on Major OSes

Windows*	• Windows* 8.1 and Windows* Server 2012 R2 include inbox driver • Open source driver in collaboration with OFA
Linux*	• Native OS driver since Linux* 3.3 (Jan 2012)
Unix	• FreeBSD driver upstream; ready for release
Solaris*	• Solaris driver will ship in S12
VMware*	• vmklinux driver certified release in Dec 2013
UEFI	• Open source driver available on SourceForge

Native OS drivers already available, with more coming!

Windows* Open Source Driver Update

Release 1 **Q2 2012**	• 64-bit support on Windows* 7 and Windows Server 2008 R2 • Mandatory features
Release 1.1 **Q4 2012**	• Added 64-bit support Windows 8 • Public IOCTLs and Windows 8 Storport updates
Release 1.2 **Aug 2013**	• Added 64-bit support on Windows Server 2012 • Signed executable drivers
Release 1.3 ***Q4 2013***	• Will add 32-bit support on all supported OS versions • End-to-end data protection

Three major open source releases since 2012.

Contributors include Huawei, PMC-Sierra*, Intel, LSI* & SanDisk**

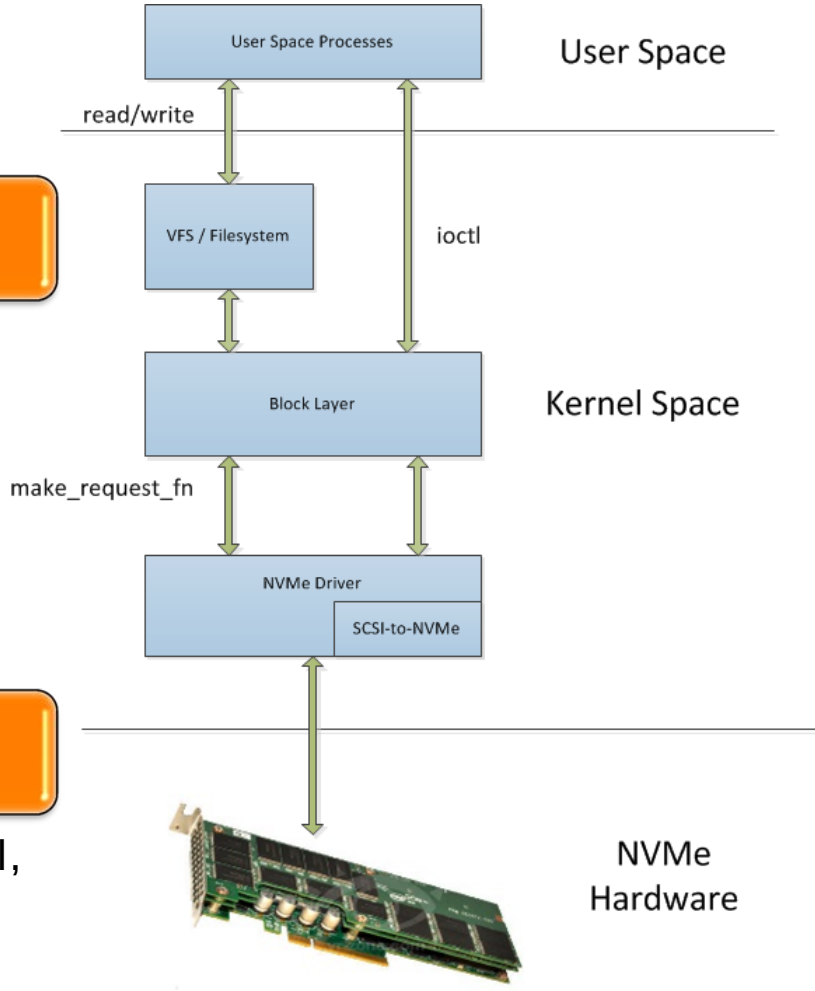
Linux* Driver Update

Recent Feature Additions

- Latest driver on Linux* 3.10
- Deallocate (i.e., Trim support)
- 4KB sector support (in addition to 512B)
- SCSI IOCTL support
- MSI support (in addition to MSI-X)
- Disk I/O statistics

Community Effort

- Contributions from Fastor*, PMC-Sierra*, Intel, Linaro*, Oracle*, SanDisk* and Trend Micro*
- 59 changes since integrated into kernel



Work in progress: power management, end-to-end data protection, sysfs manageability & NUMA optimizations

FreeBSD Driver Update

- NVM Express* (NVMe) support is upstream in the head and stable/9 branches
- FreeBSD 9.2 will be the first official release with NVMe support, slated for September

FreeBSD NVMe Modules

nvmecontrol

User space utility, including firmware update

nvd

NVMe/block layer shim

nvme

Core NVMe driver

Solaris* Driver Update

- Current Status from Oracle* team:
  - Stable and efficient working prototype conforming to 1.0c
  - Direct block interfaces bypassing complex SCSI code path
  - NUMA optimized queue/interrupt allocation
  - Support 8K memory page size on SPARC system
  - Plan to validate driver against Oracle SSD partners
  - Plan to integrate into S12 and a future S11 update release

- Future Development Plans:
  - Boot & install on SPARC and X86
  - Surprise removal support
  - Multi-path support, SR-IOV, scatter/gather lists (SGLs)

VMware Driver Update

- Initial “vmklinux” based driver in final stages of development
  - First release in mid-Oct, 2013
  - Certified release in Dec, 2013

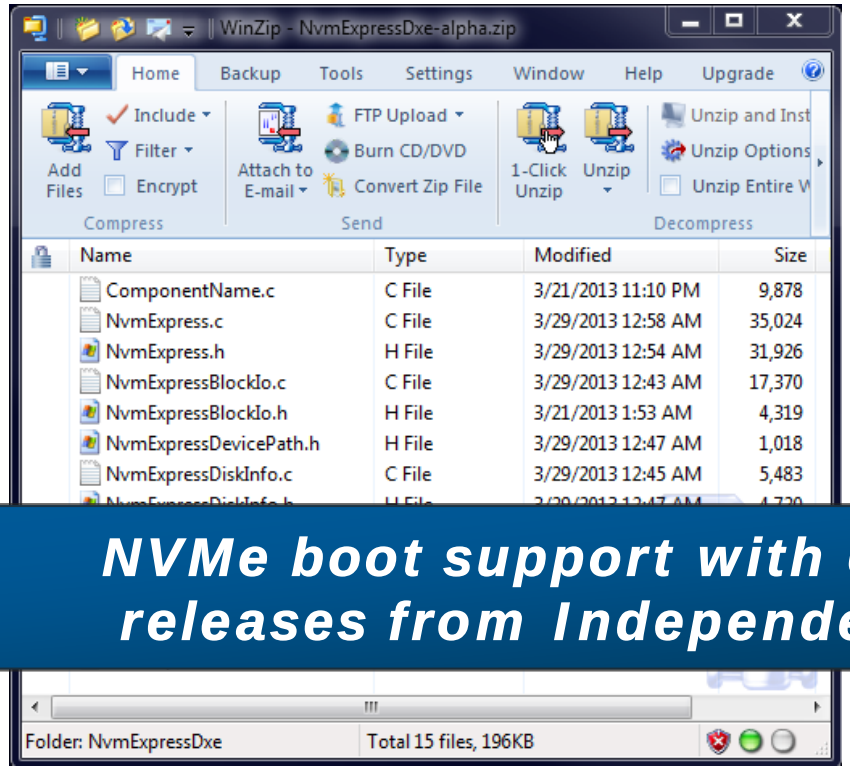
- A native VMware* NVM Express* driver is targeted for inclusion in vSphere* in 2014

- VMware‘s IOVP program includes workflow for bugs/issues

UEFI Driver Update

- The UEFI 2.4 specification available at www.UEFI.org contains updates for NVM Express* (NVMe)

- An open source version of an NVMe driver for UEFI is available at nvmexpress.org/resources



"AMI is working with vendors of NVMe devices and plans for full BIOS support of NVMe in 2014."

Sandip Datta Roy
VP BIOS R&D, AMI

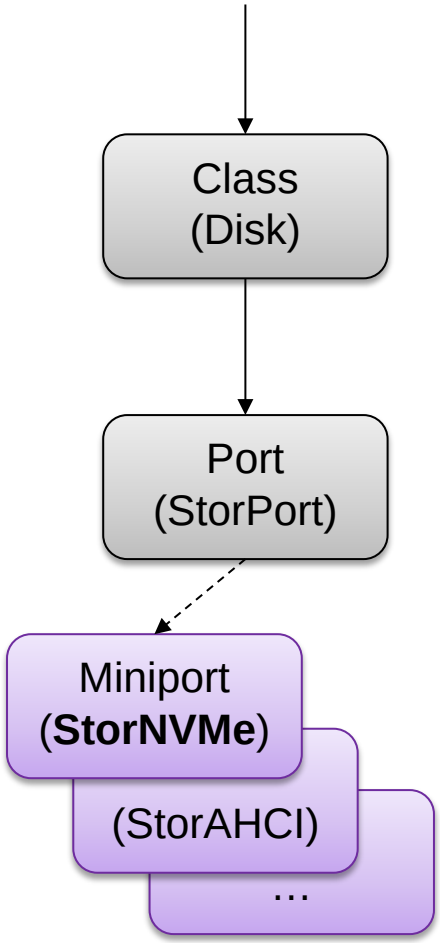
NVMe boot support with UEFI will start percolating releases from Independent BIOS Vendors in 2014

Microsoft's Support of NVMe

Robin Alexander, Microsoft

Microsoft's Support of NVM Express

- The Natural Progression from SATA for NVM
  - Standardized PCI Express* Storage
  - First devices are enterprise-class
  - High-Density / High-Performance
  - Closing the latency gap with RAM
- Windows* Inbox Driver (StorNVMe.sys)
  - Windows Server 2012 R2 (enterprise)
  - Windows 8.1 (client)
  - Stable Base Driver
- The Storport Model
  - Reduced development cost
    - Offloads Basics: PnP, Power, Setup, Crash, Boot*
  - Mature / Optimized for performance
  - RAM-backed NVMe device
    - > 1 million IOPS with < 20µs latencies



StorNVMe Delivers a Great Solution

- StorNVMe Implementation Highlights
  - Uses hardened Enterprise Storage Stack
  - Strives for 1:1 mapping of queues to processors
  - NUMA optimized
  - Asynchronous notification supported
  - Interrupt coalescing supported
  - Rigorous testing on Windows*
  - Firmware Update/Download (via IOCTL)

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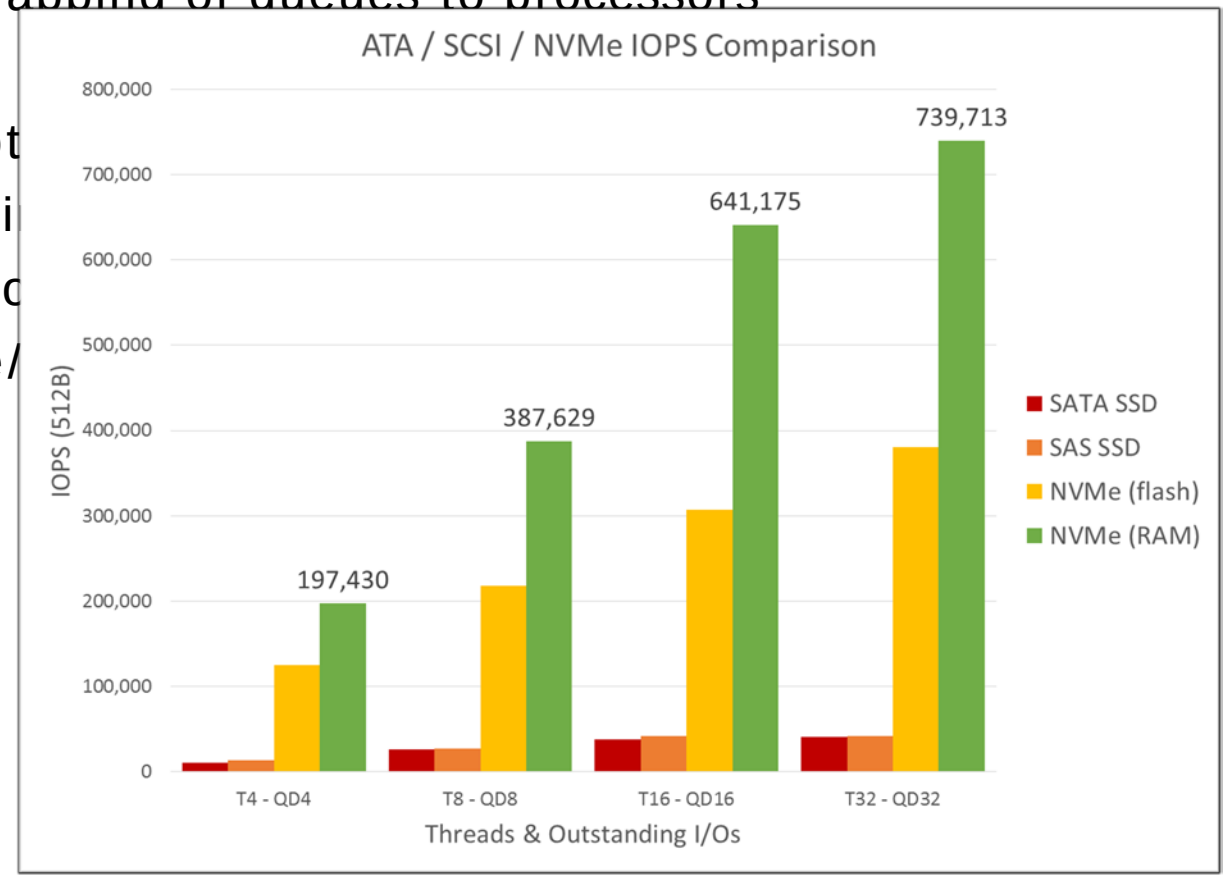

System Configuration: 2 Socket Romley-based Server, 16 physical processors (32),
Random Read Workload, Tool: IOmeter

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- With great IOPs
- And low latency

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NVMe Futures

- Microsoft is committed to NVMe
- Enterprise
  - Shareable Devices
    - High Availability (Clustering)
    - Fault Tolerance (Storage Spaces)
  - Form Factor
    - Small Devices, High Density, Transition
- Client ecosystem emerging
  - Boot requires UEFI/platform support first
  - Granular Power Management support needed in devices
  - SATA => NVMe transition is cloudy

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NVM Express* Deployment is Starting

- First plugfest held May 2013 with 11 companies participating
  - Three devices on Integrator's List
  - Next plugfest planned for Q4

- Samsung announced first NVM Express* (NVMe) product in July

FOR IMMEDIATE RELEASE

NVM Express Workgroup Holds First Plugfest

Milestone in Process to Deliver Standards-based Interoperability for PCI Express Solid-State Drives

WAKEFIELD, Mass., May 29, 2013 – The NVM Express Workgroup, developer of the NVM Express specification for accessing solid-state drives (SSDs) on a PCI Express (PCIe) bus, held its first Plugfest at the University of New Hampshire InterOperability Lab in Durham, N.H., May 13-16, 2013. This event provided an opportunity for participants to measure their products' compliance with the NVM Express (NVMe) specification and to test interoperability with other NVMe products.

The NVMe specification defines an optimized register interface, command set and feature set for PCIe-based Solid-State Drives (SSDs). NVM refers to non-volatile memory, as used in SSDs. The goal of NVMe is to unlock the potential of PCIe SSDs now and in the future, and to standardize the PCIe SSD interface. Participating in the Plugfest were Agilent Technologies, Dell Inc., Fastor Systems, Inc., HGST, a Western Digital company, Integrated Device Technology, Inc., Intel Corporation, Samsung Electronics Co., Ltd., SanDisk Corporation., sTec, Inc., Teledyne LeCroy, and Western Digital Corporation.

STORAGE REVIEW.COM

JULY 18TH, 2013 by Josh Linden

Samsung Announces Industry's First 2.5-Inch NVMe SSD

Tweet 4 Share

Samsung has announced the XS1715, a 2.5-inch Non-Volatile Memory Express (NVM Express) PCIe SSD. According to Samsung, the 1.6TB SFF-8639 NVMe SSD provides a sequential read speed at 3,000MB/s, six times faster than the company's current high-end enterprise SSD. The XS1715's random read performance is specified at up to 740,000 IOPS, more than 10 times as fast as existing SSD options.

NVMe products targeting Datacenter shipping this year

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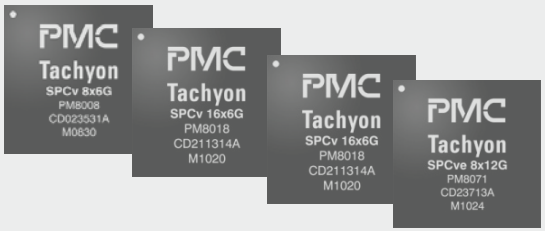
Enabling NVMe Solutions

Derek Dicker, PMC

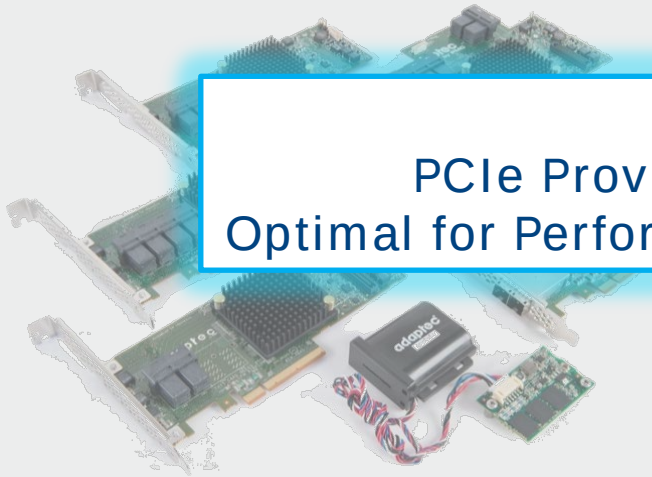
PMC Adds NVMe Products to Enterprise Storage Portfolio



Tachyon SAS Protocol Controllers

SAS Expanders

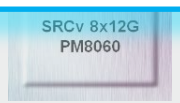
PCIe SSD Controllers



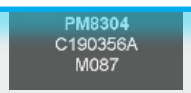
RAID Adapters & HBAs

Why?

PCIe Provides a Great Interface for SSDs,
Optimal for Performance / Latency-Sensitive Storage Tier



RAID on Chip (RoC) SAS Controllers



SAS SSD Controllers

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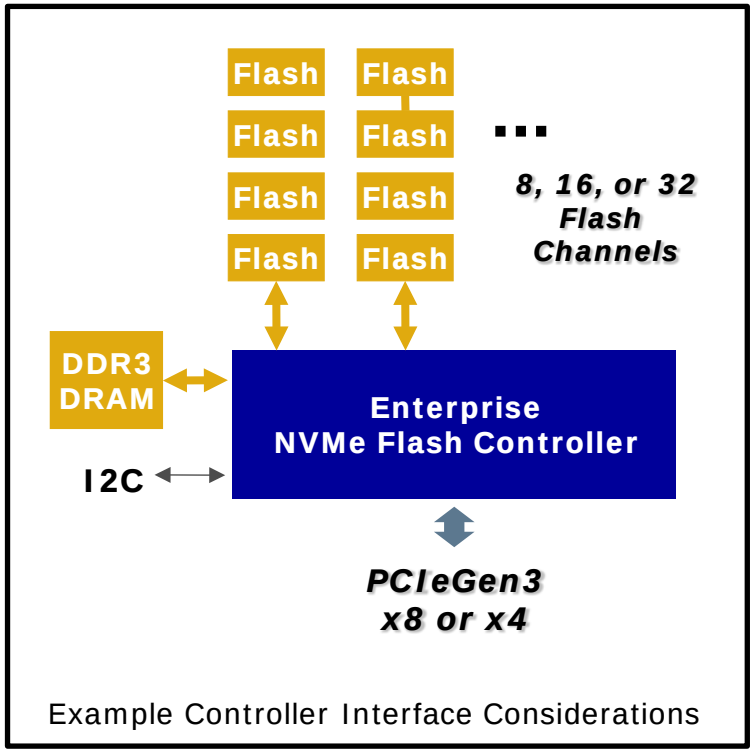
Broad Array of NVMe Products Enabled by Highly Programmable & Flexible Controllers

Controller Considerations

- NVMe Host Interface
- PCIe Gen3 Interface Configurations
  - Dual Independent Host Port Support
  - x4 or x8 Options on Single Port
- Extensible Flash Channel Support
- Broad NAND Flash Support
  - SLC, MLC, eMLC Support…Toggle & ONFI
- Encryption Capability
- Advanced Data Integrity and Reliability
- Flexible Form Factor Support



Example Controller Interface Considerations

Applications

- PCIe 2.5” Solid State Drives
- PCIe Flash Adapters
- PCIe NV-RAM Cards

NVMe Solutions On the Horizon

- Flash Solutions
  - 2.5” SSDs
  - PCIe Standard Form Factors
- NVMe Implementers
  - Tier 1 NAND Vendors
  - Tier 1 SSD Vendors
  - Tier 1 HyperScale Datacenters
  - Tier 1 OEMs
  - All Flash Appliance Vendors
- NV-RAM Solutions
  - PCIe Standard Form Factors

The World’s First Enterprise NVMe PCIe Solutions Are Forecasted to Ship in Q4!

Real NVMe Solutions

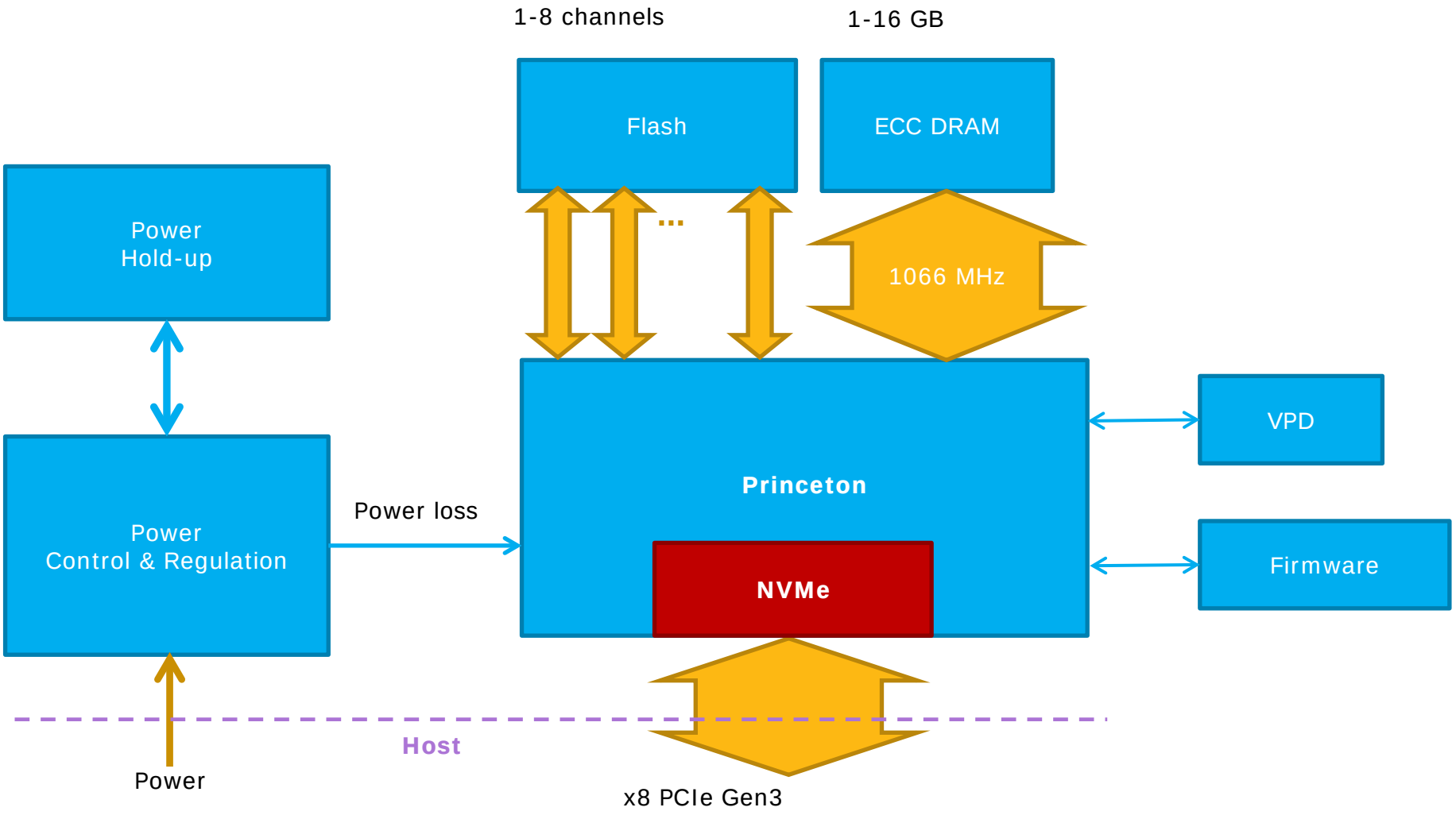
Steve Sardella, EMC

EMC's First Use of NVMe

- Aside from the obvious use case of Flash-based SSDs, NVM Express can support other applications
- One storage industry example is Non-Volatile RAM
  - Useful for journaling, logging, write caching
  - DRAM provides lower latency, higher bandwidth than Flash

Traditional NVRAM Card Implementation	Using NVM Express to Implement NVRAM
Select "generic" micro-controller with desired physical interfaces (PCIe, DRAM, Flash)	Start with an NVMe standard controller and reference firmware
Create custom software driver from scratch	Port NVMe driver/utilities, minimize firmware/software customizations
Validate in a vacuum	Leverage interoperability testing, reduce development/validation time

EMC NVRAM Hardware



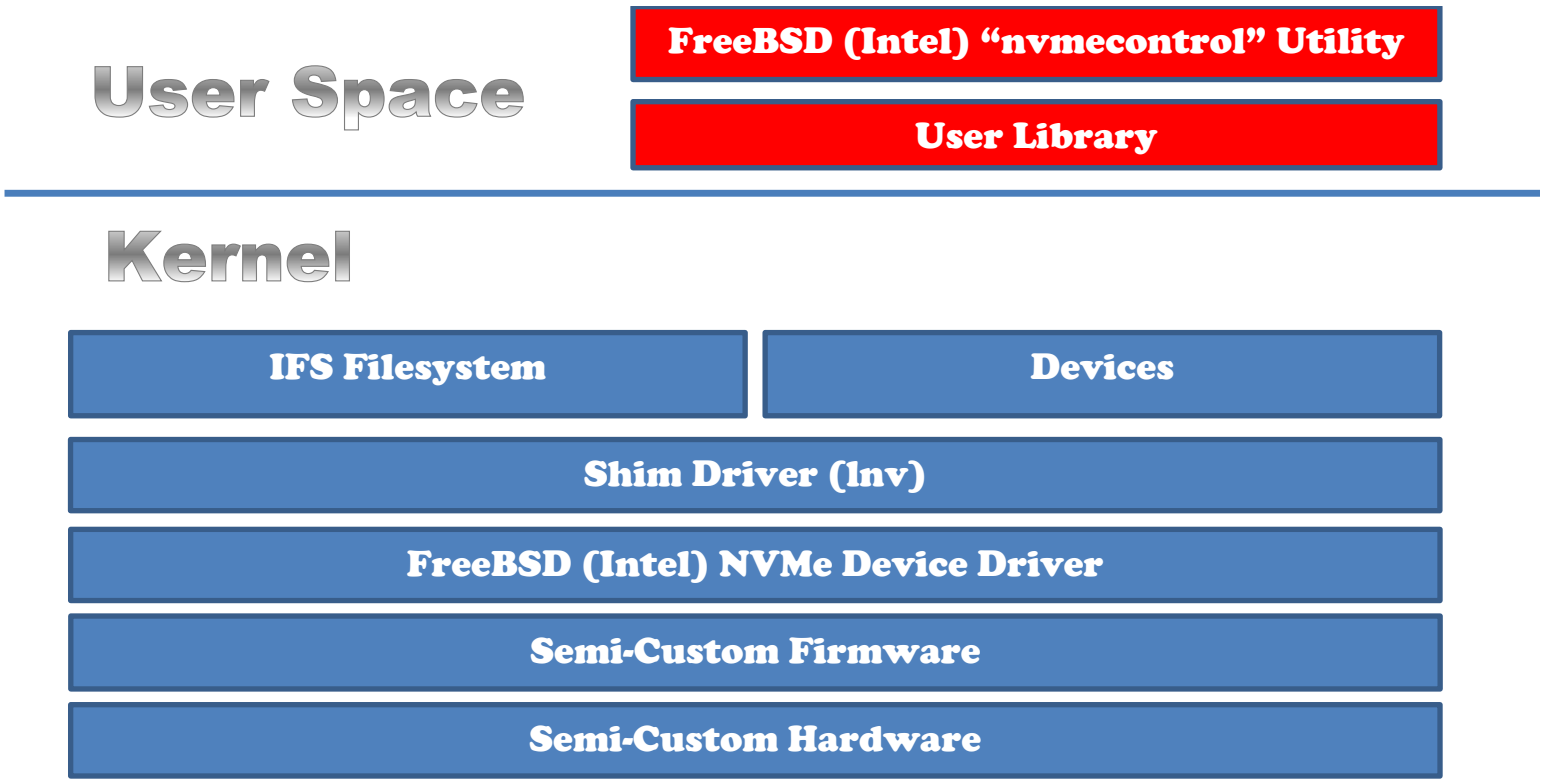
EMC NVRAM Software

NVM Express Benefits:

Allows partitioning of NVRAM into multiple namespaces for different purposes, maximizing capacity utilization

Supports multiple size LBAs, maximizing flexibility

Provides optional metadata and end-to-end data protection capabilities, maximizing robustness



The Difference a Standard Makes

- EMC and Intel engineers iteratively collaborated on the FreeBSD driver
  - EMC got off to a quick start, benefiting from previous validation work on the driver
  - Intel used EMC's design as an additional validation vehicle, and EMC engineers submitted code changes and bug fixes, to further improve the driver's robustness
- Higher performance was achieved, due to NVMe's interrupt coalescing and multiple I/O queues
- The existence of a standard saved EMC months of software development and validation, and will allow the hardware to be supported in multiple OS environments

NVM Express: "It's not just for SSDs"

For a live demo,
visit EMC at booth #728 in the NVMe Community

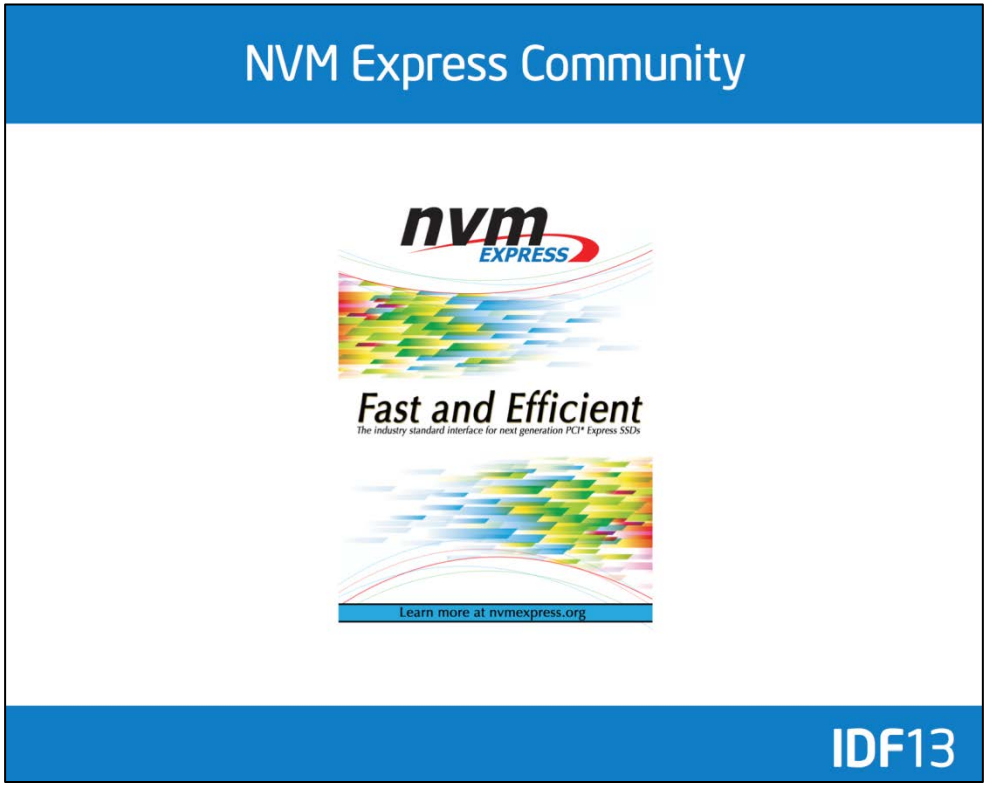
Summary

- NVM Express* is the interface architected for NAND today and next generation NVM of tomorrow
- NVM Express continues to add features to meet the needs of client and Enterprise market segments as they evolve
- The first plugfest was held in May 2013 with 11 companies participating, next plugfest in Q4
- NVMe products are starting to ship NOW!

Learn more at nvmexpress.org

Learn More in the NVMe Community

Check out the NVMe Community in the Showcase to see NVMe products in action



Company	Booth #
Dell	726
Intel	727 & 734
EMC	728
Micron	729
SanDisk	730
LSI	731
SNIA	732
PMC-Sierra	733
Agilent	735
Western Digital	736
Teledyne LeCroy	737
Viking Technology	738
Tektronix	739

Additional Sources of Information

PDF of this presentation is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. The URL is on top of Session Agenda Pages in Pocket Guide.

- Additional info in the NVMe community – booths 726 to 739
- More web based info: nvmexpress.org

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Rev. 7/17/13

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