NVM Express Technical Errata

Errata ID	**001**
Affected Spec Ver.	**NVM Express 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	2/9/2011

This erratum addresses several items.

The marketing name of the specification has been selected to be “NVM Express”. All instances of “Enhanced NVMHCI” in the specification need to be replaced with the new name.

There is a typo in the PRP Entry 1 definition where “log page” should refer instead to the “Identify data structure”.

In the Identify Controller data structure, some clarifications should be added for Submission Queue Entry Size and Completion Queue Entry Size for the NVM Command Set. Specifically, the maximum values need clarification that a larger value than the required may be specified for proprietary extensions.

For the namespace, the erratum clarifies that the namespace identifiers shall start at 1. The value of 0 for namespace ID is a value that indicates that the namespace ID is not used for the command.

Description of the specification technical flaw

Throughout the specification, make the following change:

Change instances of “Enhanced NVMHCI” to “NVM Express”.

Modify Figure 62 as shown below:

Figure 62: Identify – PRP Entry 1

Bit	Description
63:00	**PRP Entry 1 (PRP1):** Indicates a data buffer that the ~~log page~~ Identify data structure shall be returned to. The buffer shall not have more than one physical discontinuity and shall be 4KB minimum in size.

Modify Figure 65 as shown below:

NVM Command Set Attributes		
512	M	**Submission Queue Entry Size (SQES):** This field defines the required and maximum Submission Queue entry size when using the NVM Command Set. Bits 7:4 define the maximum Submission Queue entry size when using the NVM Command Set. This value is larger than or equal to the required SQ entry size. The value is in bytes and is reported as a power of two (2^*n*). The recommended value is 6, corresponding to a standard NVM Command Set SQ entry size of 64 bytes. Controllers that implement proprietary extensions may support a larger value. Bits 3:0 define the required Submission Queue Entry size when using the NVM Command Set. This is the minimum entry size that may be used. The value is in bytes and is reported as a power of two (2^*n*). The required value shall be 6, corresponding to 64.
513	M	**Completion Queue Entry Size (CQES):** This field defines the required and maximum Completion Queue entry size when using the NVM Command Set. Bits 7:4 define the maximum Completion Queue entry size when using the NVM Command Set. This value is larger than or equal to the required CQ entry size. The value is in bytes and is reported as a power of two (2^*n*). The recommended value is 4, corresponding to a standard NVM Command Set CQ entry size of 16 bytes. Controllers that implement proprietary extensions may support a larger value. Bits 3:0 define the required Completion Queue entry size when using the NVM Command Set. This is the minimum entry size that may be used. The value is in bytes and is reported as a power of two (2^*n*). The required value shall be 4, corresponding to 16.
515:514		Reserved
519:516	M	**Number of Namespaces (NN):** This field defines the number of valid namespaces present for the controller. Namespaces shall be allocated in order (starting with ~~0~~ 1) and packed sequentially. ~~This is a 0's based value.~~

Modify the first paragraph of section 6.1 as shown below:

6.1 Namespaces

A namespace is a collection of logical blocks that range from 0 to the capacity of the namespace – 1. The number of namespaces present is reported in the Identify Controller data structure. The namespaces are allocated in order (starting with ~~0~~ 1) and packed sequentially. Namespaces identifiers may change across power off conditions. The management (creation, deletion) of namespaces is outside the scope of this specification.

Disposition log

2/9/2011	Erratum captured.
3/15/2011	Erratum ratified.