NVM Express Technical Errata

Errata ID	**002**
Affected Spec Ver.	**NVM Express 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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This erratum addresses several items.

The Controller Configuration register as a 64-bit register is misaligned. The upper 32-bits of this register are reserved. To fix the alignment without impact to ongoing hardware implementations, this register is converted to a 32-bit register.

In the Identify command, there is reference to “command header” which should be a reference to the Namespace Identifier in Command Dword 1.

In the table describing NVM Command Set specific Admin opcodes, there is a note that includes reference to Set/Get Features and Identify commands. These Admin commands are not NVM Command Set specific so that portion of the note is removed.

Description of the specification technical flaw

Modify section 3.1 as shown below:

The following table describes the register map for the controller.

Start	End	Symbol	Description
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h ~~1Bh~~	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1004h	1007h	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
1008h	100Bh	SQ1TDBL	Submission Queue 1 Tail Doorbell
100Ch	100Fh	CQ1HDBL	Completion Queue 1 Head Doorbell
1010h	1013h	SQ2TDBL	Submission Queue 2 Tail Doorbell
1014h	1017h	CQ2HDBL	Completion Queue 2 Head Doorbell
…	…	…	…
1000h+ (8*y)	1003h + (8*y)	SQyTDBL	Submission Queue y Tail Doorbell
1004h+ (8*y)	1007h + (8*y)	CQyHDBL	Completion Queue y Head Doorbell
			Vendor Specific (Optional)

Modify the Controller Configuration register in section 3.1.5 as shown below:

Bit	Type	Reset	Description
~~63~~ 31:24	RO	0	Reserved
23:20	RW	0	**I/O Completion Queue Entry Size (IOCQES):** This field defines the I/O Completion Queue entry size that is used for the selected I/O Command Set. The required and maximum values for this field are specified in the Identify Controller data structure for each I/O Command Set. The value is in bytes and is specified as a power of two (2^*n*).

Modify Figure 64 as shown below:

Figure 64: Identify – Command Dword 10

Bit	Description
31:01	Reserved
00	**Controller or Namespace Structure (CNS):** If set to '1', then the Identify Controller data structure is returned to the host. If cleared to '0', then the Identify Namespace data structure is returned to the host for the namespace specified in the Namespace Identifier (CDW1.NSID) field ~~command header~~.

Modify Figure 25 as shown below:

Figure 25: Opcodes for Admin Commands – NVM Command Set Specific

Opcode (07)	Opcode (06:02)	Opcode (01:00)	Opcode	O/M	Namespace Identifier Used[3]	Command
Generic Command	Function	Data Transfer				
1b	000 00b	00b	80h	O	Yes	Format NVM
1b	000 00b	01b	81h	O	No	Security Send
1b	000 00b	10b	82h	O	No	Security Receive

NOTES:
1. O/M definition: O = Optional, M = Mandatory.
2. Opcodes not listed are reserved.
3. A subset of commands uses the Namespace Identifier field (CDW1.NSID). When not used, the field shall be cleared to 0h. ~~For the Get Features and Set Features command, the Namespace Identifier is only used for the LBA Range Type feature. For the Identify command, the Namespace Identifier is only used for the Namespace data structure.~~

Disposition log

3/3/2011	Erratum captured.
3/7/2011	Controller Configuration register change added.
4/8/2011	Erratum ratified.